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10/774,466	02/10/2004	Shigetaka Kasuga	2004_0104A	9129

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,466	KASUGA ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernandez	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 20-23* is/are rejected.

7)☒ Claim(s) *13-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/30/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: in page 4, line 2, "generation circuit 140. ." (there are two periods (.) after "circuit 140") should read "generation circuit 140.". Also in page 6, line 6, the word" sifting" should read" shifting".

Appropriate correction is required.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-12 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoshi et al., JP 2000-078484 A in view of Applicants Admitted Prior Art (AAPA).

Regarding claim 1, Satoshi et al. discloses a solid-state image sensing apparatus (Fig. 1) that performs photoelectric conversion of incident light, comprising: a photosensitive unit (Fig. 1: 3) in which a plurality of photoelectric conversion circuits is laid out one-dimensionally or two-dimensionally (English Translation, Page 3, ¶ 0008),

each of said photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal (See fig. 2; English Translation, page 3, ¶ 0009); an electric charge simultaneous removal unit (Fig. 1: 8) operable to simultaneously remove the accumulated electric charge in the photodiodes laid out in a predetermined region to be read out in the photosensitive unit (English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016).

Satoshi et al. does not explicitly disclose an electric charge accumulation unit operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after the accumulated electric charge in the photodiode that is laid out in the region is removed.

However, AAPA discloses a solid-state image sensing apparatus (Fig. 1) that performs photoelectric conversion of incident light, comprising: a photosensitive unit (See fig. 1) in which a plurality of photoelectric conversion circuits (Fig. 1: 112) is laid out one-dimensionally or two-dimensionally, each of said photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal; an electric charge removal unit (timing generation unit) operable to remove the accumulated electric charge in the photodiodes laid out in a predetermined region to be read out in the photosensitive unit; and an electric charge accumulation unit (Fig. 2: 128) operable to

accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after the accumulated electric charge in the photodiode that is laid out in the region is removed (Page 1, lines 11-32; page 2, line 1 – page 6, line 1).

Therefore, taking the combined teaching of Satoshi et al. in view of AAPA as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Satoshi et al. by having an electric charge accumulation unit operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after the accumulated electric charge in the photodiode that is laid out in the region is removed. The motivation to do so would have been to allow the photodiode to start collecting new signal charge while reading out image signal and would also allow the image sensor to accumulate more image signal to increase the dynamic range of the image.

Regarding claim 2, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge accumulation unit generates an electric accumulation start signal to start electric charge accumulation to the photodiode laid out in the region to be read out (After the reset signal is made, the exposure starts by opening a shutter (Fig. 1: 2) to have the pixels accumulate charge signal; See Satoshi et al., English Translation, page 4, ¶ 0011 – page 5, ¶ 0016; see also AAPA, Page 1, lines 11-32; page 2, line 1 – page 3, line 2).

Regarding claim 3, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge accumulation unit generates an electric accumulation end signal and ends electric charge accumulation to

the photodiode laid out in the region to be read out in response to activation of the electric charge accumulation end signal (After the exposure signal is made, a signal to close a mechanical shutter (Fig. 1: 2) to stop accumulating image signal and the accumulated signal is read; See Satoshi et al., English Translation, page 4, ¶ 0011 – page 5, ¶ 0016; see also AAPA, Page 1, lines 11-32; page 2, line 1 – page 3, line 2).

Regarding claim 4, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches an incident light control unit (Satoshi et al., CPU 8 controls the mechanical shutter 2; see fig. 1) operable to control incidence of light into the photosensitive unit, wherein the electric charge accumulation unit ends electric charge accumulation to the photodiode laid out in the region to be read out using the incident light control unit by blocking out incidence of light into the photosensitive unit (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016).

Regarding claim 5, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches an incident light control unit (Satoshi et al., CPU 8 controls the mechanical shutter 2; see fig. 1) operable to control incidence of light into the photosensitive unit, wherein the electric charge accumulation unit starts incidence of light to the photosensitive unit using the incident light control unit after the electric charge simultaneous removal unit simultaneously removes the accumulated electric charge to the photodiode laid out in the region to be read out (After the reset signal is made, the exposure starts by opening a shutter (Satoshi et al., fig. 1: 2) to have the pixels accumulate charge signal and after the exposure signal is made, a signal to

close a mechanical shutter (Satoshi et al., fig. 1: 2) to stop accumulating image signal and the accumulated signal is read; Satoshi et al., English Translation, page 4, ¶ 0011 – page 5, ¶ 0016).

Regarding claim 6, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge accumulation unit generates an electric accumulation end signal and ends electric charge accumulation to the photodiode laid out in the region to be read out in response to activation of the electric charge accumulation end signal (See AAPA, page 2, lines 9-30).

Regarding claim 7, limitations can be found in claim 4.

Regarding claim 8, the combined teaching of Satoshi et al. in view of AAPA fails to teach that the incident light control unit includes: a liquid crystal shutter that is set up between the photosensitive unit and an object to be photographed; and a liquid crystal shutter control unit operable to apply a predetermined voltage to the liquid crystal shutter to control penetration of light.

However, Official Notice is taken that the use of liquid crystal shutter set up between the photosensitive unit and an object to be photographed controlled by applying a predetermined voltage to the liquid crystal shutter to control penetration of light is well known in the art and one of an ordinary skill in the art would be motivated to change the mechanical shutter in Satoshi et al. with a liquid crystal shutter with the motivation of reducing the power drain of the mechanical shutter and also to reduce the complexity and size of the imaging device.

Regarding claim 9, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge simultaneous removal unit simultaneously outputs a reset signal to all the photoelectric conversion circuits laid out in the region to be read out (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016; see also AAPA, Page 1, lines 11-32; page 2, line 1 – page 3, line 2); and the output circuit in the photoelectric conversion circuit includes: a first transistor (Fig. 3: 24) that receives the reset signal from the electric charge simultaneous removal unit and that resets electric charge accumulated in the photodiode in response to activation of said reset signal (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016); and a second transistor (Fig. 3: 22) that lets the electric signal pass through, the electric signal according to value of voltage determined by electric charge outputted from the photodiode (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016; see also AAPA, Page 1, lines 11-32; page 2, line 1 – page 3, line 2).

Regarding claim 10, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches the electric charge simultaneous removal unit generates a gate signal (A gate signal is inherent to activate the reset transistor 24 in Satoshi et al.) and includes a reset signal passage switch (Fig. 2: 19, OR circuit used to activate or deactivate the reset signal) that outputs simultaneously the reset signal to all the photoelectric conversion circuits in response to activation of the gate signal (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016).

Regarding claim 11, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge simultaneous removal unit includes: a switch transistor (AAPA; fig. 3: 148) that serves as a switch; and a capacitor (AAPA, fig. 3: 146) that is set up between a gate and a source or a drain of the switch transistor, and when the capacitor is charged, the reset signal is inputted from the drain of the switch transistor and is outputted simultaneously to all the photoelectric conversion circuits from the source (the teaching of Satoshi et al. as modified with the AAPA reference would provide the reset signal is inputted from the drain of the switch transistor and is outputted simultaneously to all the photoelectric conversion circuits from the source; Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016; see also AAPA, Page 1, lines 11-32; page 2, line 1 – page 3, line 2).

Regarding claim 12, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge simultaneous removal unit outputs a readout signal simultaneously and outputs a reset signal to all the photoelectric conversion circuits laid out in the region to be read out (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016), and the output circuit in the photoelectric conversion circuit includes: a first transistor (AAPA, fig. 2: 124) that receives the readout signal from the electric charge simultaneous removal unit (Satoshi et al. fig. 1: 8, AAPA, fig. 3) and lets the electric charge accumulated in the photodiode (Satoshi et al., fig. 3: 21; AAPA, fig. 2: 122) pass through in response to activation of the readout signal; and an electric charge retention unit (AAPA, fig. 2: 128)

operable to receive the electric charge that passes through the first transistor and retain said electric charge ; a second transistor (Satoshi et al., fig. 3: 22; AAPA, fig. 2: 130) that lets the electric signal pass through, the electric signal according to value of voltage determined by the electric charge retained by the electric charge retention unit; and a reset circuit (AAPA, fig. 2: 19) that receives the reset signal from the electric charge simultaneous removal unit and that resets an amount of electric charge accumulated in the electric charge retention unit in response to activation of the reset signal (Satoshi et al., English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016; AAPA, Page 1, lines 11-32; page 2, line 1 – page 6, line 1).

Regarding claim 20, the combined teaching of Satoshi et al. in view of AAPA as discussed and analyzed in claim 1, teaches that the electric charge simultaneous removal unit generates a gate signal and includes a readout signal passage switch that outputs simultaneously the readout signal to all the photoelectric conversion circuits in response to the gate signal (although AAPA does not teach performing the simultaneous readout, the teaching of Satoshi et al. as modified with the AAPA reference would provide the electric charge simultaneous removal unit generating a gate signal and includes a readout signal passage switch that outputs simultaneously the readout signal to all the photoelectric conversion circuits in response to the gate signal AAPA, page 3, line 3 – page 4, line 2).

Regarding claim 21, limitations can be found in claim 11.

Regarding claim 22, Satoshi et al discloses a camera (Fig. 1) that photographs an object comprising a solid-state image sensing apparatus (Fig. 1: 3); and a

mechanical shutter (Fig. 1: 2), wherein the solid-state image sensing apparatus includes: a photosensitive unit (Fig. 2) in which a plurality of photoelectric conversion circuits (Fig. 2: 11) is laid out one-dimensionally or two-dimensionally, each of said photoelectric conversion circuits corresponding to a pixel and including a photodiode (Fig. 3: 21) that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal; an electric charge simultaneous removal unit (Fig. 1: 8) operable to simultaneously remove the accumulated electric charge in the photodiode laid out in a predetermined region to be read out in the photosensitive unit; and an incident light control unit (Fig. 1: 8, CPU 8 controlling the mechanical shutter 2) operable to control incidence of light into the photosensitive unit, wherein the mechanical shutter is set up between the photosensitive unit of the solid-state image sensing apparatus and an object to be photographed (See fig. 1), the photodiode ends electric charge accumulation in the region to be read out using the incident light control unit by blocking out incidence of light into the photosensitive unit (English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016), and the incident light control unit controls incidence of light into the photosensitive unit by controlling opening and shutting of the mechanical shutter (English Translation, page 3, ¶ 0008-0009; page 4, ¶ 0011 – page 5, ¶ 0016).

Satoshi et al. does not explicitly disclose an electric charge accumulation unit operable to accumulate electric charge in the photodiode laid out in the region to be

read out during a predetermined time after accumulated electric charge in the photodiode that is laid out in the region is removed.

However, AAPA discloses a solid-state image sensing apparatus (Fig. 1) that performs photoelectric conversion of incident light, comprising: a photosensitive unit (See fig. 1) in which a plurality of photoelectric conversion circuits (Fig. 1: 112) is laid out one-dimensionally or two-dimensionally, each of said photoelectric conversion circuits corresponding to a pixel and including a photodiode that accumulates electric charge by performing the photoelectric conversion of incident light and an output circuit that outputs the accumulated electric charge as an electric signal; an electric charge removal unit (timing generation unit) operable to remove the accumulated electric charge in the photodiodes laid out in a predetermined region to be read out in the photosensitive unit; and an electric charge accumulation unit (Fig. 2: 128) operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after the accumulated electric charge in the photodiode that is laid out in the region is removed (Page 1, lines 11-32; page 2, line 1 – page 6, line 1).

Therefore, taking the combined teaching of Satoshi et al. in view of AAPA as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Satoshi et al. by having an electric charge accumulation unit operable to accumulate electric charge in the photodiode laid out in the region to be read out during a predetermined time after accumulated electric charge in the photodiode that is laid out in the region is removed. The motivation to do so would have been to allow the photodiode to start collecting new signal charge while reading out

image signal and would also allow the image sensor to accumulate more image signal to increase the dynamic range of the image.

Regarding claim 23, claim 23 is a method claim of the apparatus in claim 1. Limitations have been discussed and analyzed with respect to claim 1.

Allowable Subject Matter

5. **Claims 13-19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 13, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest an electric signal readout unit operable to read out the electric signal outputted from the photoelectric conversion circuit laid out in the region to be read out, wherein the electric signal readout unit includes: a first unit operable to output the activated reset signal to the reset circuit in the photoelectric conversion circuit laid out in the region to be read out; and a second unit operable to output the activated readout signal to said reset circuit after outputting said reset signal, and the first unit outputs the reset signal activated after the predetermined time in the electric charge accumulation unit has passed including all the limitations of claims 1 and 12.

Regarding claim 17, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest an electric signal readout unit operable to read out the electric signal outputted from the photoelectric conversion circuit laid out in the region to be read out, wherein the electric signal readout unit includes: a first unit operable to output the activated reset signal to the reset circuit in the photoelectric conversion circuit laid out in the region to be read out; and a second unit operable to output the activated readout signal to said reset circuit after outputting said reset signal, and the first unit outputs the reset signal activated before the predetermined time in the electric charge accumulation unit has passed including all the limitations of claims 1 and 12.

Regarding claim 19, the main reason for indication of allowable subject matter is because the prior art fails to teach or reasonably suggest an electric signal readout unit operable to read out the electric signal outputted from the photoelectric conversion circuit laid out in the region to be read out, wherein the electric signal readout unit includes: a first unit operable to output the activated reset signal to the reset circuit in the photoelectric conversion circuit laid out in the region to be read out; and a second unit operable to output the activated readout signal to said reset circuit after outputting said reset signal, and the first unit outputs the activated reset signal for a period since some mid point of the predetermined time until an end of said predetermined time in the electric charge accumulation unit including all the limitations of claims 1 and 12.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernandez whose telephone number is (571) 272-7311. The examiner can normally be reached on 8:30 A.M. to 6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571) 272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nelson D. Hernandez
Examiner
Art Unit 2622

NDHH
May 25, 2007

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